DOMINANCE OF THE DIGITAL (1990–2016)

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PLAN FOR TODAY

A. *Leonardo to the Internet*: chapter = ‘era’

B. Method: ‘levels of analysis’ + tech determinism

   1. Moore’s Law . . . explains ‘all’ but where/how?
   2. ‘Silicon Valley’ as global innovation model
   3. Convergence in/across industries + users
   4. *Compare* China and US: *different* socio-economies . . . why ‘similar’ tech outcomes?
• *L2i* is ‘big’ history but with narrative on places, people, institutions, situated processes (not disembodied ‘indus rev’ or ‘global economy’)

• Emerging socio-technical structures* ‘select’ certain technologies . . . entrenched (for a time)

• Eras [⇒] narrate dominant institutions (e.g. courts 1450+, commerce, industry, empire, . . .)
<table>
<thead>
<tr>
<th>Court</th>
<th>Commerce</th>
<th>Industry</th>
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</thead>
<tbody>
<tr>
<td>Empire</td>
<td>Science &amp; Systems</td>
<td>Modernism</td>
</tr>
<tr>
<td>War</td>
<td>Global Economy</td>
<td>Systemic Risk</td>
</tr>
</tbody>
</table>

B. METHOD

• Social construction vs technical shaping:
  - Micro: T shaped by society, politics, economy
  - Meso: interactions S + T
  - Macro: T shapes society, politics, economy [TD]

• ‘Levels of analysis’:
  - Micro: diversity, indeterminacy, agency
  - Meso: ‘in between’ processes, aggregations
  - Macro: patterns, outcomes, structures

B. METHOD

- Is ‘Moore’s Law’ instance of T determinism?
  - P. Ceruzzi T&C (2005) ‘ML and T Determinism’
  - Snapshots ‘library cards’/DVDs; chalk/cellphone: thus ‘Moore’s law is at work’
  - Affirms … ‘raw technological determinism’

- And today’s fears: automation, AI, IOT . . . ??

- Misa here: not ‘snapshots’ but narrative+process
  - Preconditions for ML (pre-1975)
  - Emergence & shaping of ML (1975–2004)
  - Institutional ‘roadmapping’ and R&D synch
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip.

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

...
C. MOORE’S LAW: VIEWS (2)

Electronics

19 April 1965
C. MOORE'S LAW: VIEWS (3)

TI integrated circuit (early 1960s)  Pentium-4 300mm wafer (2000)

‘snapshots’ create TD!
D. MOORE’S LAW: NARRATIVE

- 1960s: US semiconductor [s.c.] industry: cut-throat capitalism, no trust, anti-cooperative
- ~12% components were defective == no IC’s
- Enter: Univac’s QC (1966-) S.C. Control Facility (1973-86): detailed failure data on s.c. vendors
- Made visible ‘meso’ level = US s.c. vendors (TI, Motorola, Fairchild … all but IBM); created standard, objective measures of industry-wide failure rates: industry averages + each-company
- ++QC precondition for IC’s >100 elements
D. MOORE’S LAW: NARRATIVE


• G. Moore “Cramming More Components onto Integrated Circuits” *Electronics* (1965)
• R. Noyce “Large Scale Integration: What is Yet to Come?” *Science* (1977)
• R. Noyce “Microelectronics” *Scientific Am* (1977)
• Carver Mead’s Caltech-based evangelism (using Moore’s devices and data)
✓ Already industry-wide efforts Univac et al
✓ Rising Japan’s s.c. industry as threat


• SEMATECH f. 1987 (14 US firms + $500M DoD)
  ▶ Cooperative R&D across s.c. industry!
  ▶ IBM leads ‘roadmapping’ inside SEMATECH
• Semiconductor Industry Assoc [SIA] (f. 1977) starts (similar) National Technology Roadmap for Semiconductors (NTRS)

• 1992 et seq reports with 15-year forecasts of transistor size, lithography [needed wavelength], interconnects, testing, factory integration

• ‘If we can stay on the SIA Roadmap, we can essentially stay on the [Moore’s Law] curve. It really becomes a question of putting the track ahead of the train to stay on plan.’ (G. Moore ’97)
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<tr>
<td>Feature size (microns)</td>
<td>0.50</td>
<td>0.35</td>
<td>0.25</td>
<td>0.18</td>
<td>0.12</td>
<td>0.10</td>
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<td>Gates per chip (millions)</td>
<td>0.3</td>
<td>0.8</td>
<td>2.0</td>
<td>5.0</td>
<td>10.0</td>
<td>20.0</td>
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<tr>
<td>Bits per chip</td>
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<td>DRAM</td>
<td>16M</td>
<td>64M</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
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<td>16M</td>
<td>64M</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
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<td>Wafer processing cost ($/cm²)</td>
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<td>3.90</td>
<td>3.80</td>
<td>3.70</td>
<td>3.60</td>
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<td>Chip size (mm²)</td>
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<tr>
<td>logic</td>
<td>250</td>
<td>400</td>
<td>600</td>
<td>800</td>
<td>1,000</td>
<td>1,250</td>
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<tr>
<td>memory</td>
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<td>200</td>
<td>320</td>
<td>500</td>
<td>700</td>
<td>1,000</td>
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<td>Wafer diameter (mm)</td>
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<td>Defect density (defects/cm²)</td>
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<td>0.01</td>
<td>0.004</td>
<td>0.002</td>
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<td>Levels of interconnect (for logic)</td>
<td>3</td>
<td>4-5</td>
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<td>5-6</td>
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<td>6-7</td>
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<td>Maximum power (watts/die)</td>
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<tr>
<td>high performance</td>
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<td>15</td>
<td>30</td>
<td>40</td>
<td>40-120</td>
<td>40-200</td>
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<tr>
<td>portable</td>
<td>3</td>
<td>4</td>
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<td>Power supply voltage</td>
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<td>desktop</td>
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<td>2.2</td>
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<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
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</table>
D. MOORE’S LAW: NARRATIVE


• NTRS ➔ International TRS (SIA’s of US, Japan, Europe, S.Korea, Taiwan)

• ITRS biennial ‘roadmaps’ 1998 … 2003 (936 companies)

• Moore’s Law as ‘self-fulfilling prediction that drives industry-wide planning’ (NSF 2000)

• ‘It’s not … a law of physics … what people are willing to let themselves believe.” (C.Mead ’05)

• Last ITRS full report in 2013. ITRS ended 2016*
E. END OF MOORE’S LAW?

- For 1965–2004 do ‘one thing’ for ever-smaller, faster, cheaper chips: **shrink their size!**
- technical trajectory created by Univac’s QC+SCF ‘ML’… SEMATECH… NTRS (1992-), ITRS (-2016)
- Intel hit ‘thermal wall’ in 2004: no longer ever-smaller sizes (= ever-faster/cheaper chips) **NYT**
E. END OF MOORE’S LAW?

Stuttering

- Transistors per chip, '000
- Clock speed (max), MHz
- Thermal design power*, w

Transistors bought per $, m

Sources: Intel; press reports; Bob Colwell; Linley Group; IB Consulting; The Economist

*Maximum safe power consumption
CONCLUSION

• Is ‘Dominance of Digital’ … T determinist?
• ML’s as ‘snapshots’ appears to be TD …
• … but narrative + process shows politics, cultural shifts, institutional innovations … connects micro/meso/macro ‘levels of analysis’
• Similar narratives + processes for:
  ‣ ‘Silicon Valley’ as global innovation model
  ‣ Convergence across industries + users
  ‣ Compare China and US internet, high-tech, AI
• Understand technology, underlying structures, interactions with politics and culture
MISA BIBLIO


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